UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,193	08/30/2006	Mohamed Azimane	US04 0145 US3	5900

65913 7590 12/07/2010

NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
MCMAHON, DANIEL F	

ART UNIT	PAPER NUMBER
2117	

NOTIFICATION DATE	DELIVERY MODE
12/07/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/591,193	AZIMANE ET AL.	
	Examiner	Art Unit	
	DANIEL F. MCMAHON	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to arguments filed September 24, 2010.

Claims 1 and 3 – 24 are pending in the application.

Response to Arguments

1. Applicant's arguments filed September 24, 2010, regarding the rejection of claims 1 and 3 – 24, under 35 U.S.C. 103(a), have been fully considered but they are not persuasive.

2. Applicant argues: The combination of cited references does not teach providing an external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern. The examiner disagrees.

Specifically, applicant argues: The Office Action, 6/24/2010, acknowledges Churchill does not teach the limitation. Additionally, the office action relies on Lackey teaching the limitation "providing the external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern".

The examiner notes the Churchill teaches "an external clock" (column 19, lines 5 – 10), as cited in the office action, 6/24/2010. Lackey is relied on for the specific teaching of: a predetermined test pattern providing the external clock signal to a plurality of different internal blocks. (column 5, lines 61 – 65; column 6, lines 10 – 16). Examiner relies on Churchill to disclose the well known design choice of an external clock.

Applicant further argues: Lackey does not teach an external clock. Specifically, applicant argues: Lackey uses a signal internal system clock and the system clock is not an external clock. The examiner disagrees.

Lackey teaches a system clock and an oscillator (figure 1). Lackey is silent as to the ultimate location of the oscillator and source of the system clock. One of ordinary skill in the art would understand in light of the teachings of Churchill that a system clock can be derived from an external source, such as an oscillator. Additionally, the disclosure of Lackey includes testing though LBIST which one of ordinary skill in the art would understand that an external clock source is a well known design choice for the purpose of testing logic without an internal clock source. Finally, Lackey discloses three functional modes, which include an external test mode that allows for external input of test data through the chip's pins. One of ordinary skill in the art would understand the combination of the external test mode and the external clock as taught by Churchill would lead to a predictable result.

3. Applicant additionally argues: Lackey teaches away from using an external clock. Specifically, Lackey teaches away from the use of multiple clocks from different clock domains that do not operate synchronously with each other (Lackey column 2, lines 7 - 19). Further, an external clock is an asynchronous clock. The examiner disagrees.

First, Lackey discloses: “It is, therefore, a primary object of the present invention to provide a generic clocking mechanism that can be applied to any clock-based logic design" (Column 2, lines 35 - 37). Additionally, Lackey discloses synchronous clock

operations (column 3, lines 21 – 22) and asynchronous clock operations (column 3, line 29). Finally, the language cited by applicant, column 2, lines 7 – 19, is contained in the background portion of the disclosure and appears to be describing problems in the prior art, which the disclosed invention has over come.

And for the reasons stated above the rejection of the claims is maintained.

Claim Rejections - 35 USC § 103 (old)

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3 – 13, and 16 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill et al. U.S. Patent 6,115,836 (herein Churchill), in view of Irrinki et al. U.S. Patent 5,822,228 (herein Irrinki), Savir U.S. Patent 5,642,362 (herein Savir), and Lackey U.S. Patent 6,467,044 (herein Lackey).

6. Regarding claim 1, Churchill teaches: A method comprising: receiving an internal clock signal (figure 9, element 916) from a clock monitor of the self-timed memory (figure 9, element 902; figure 11c, element 1102); receiving an external clock signal (figure 2, clk); receiving a control signal (figure 9, element 912); and providing, in dependence upon the control signal, the internal clock signal to at least one internal

memory block during a normal mode of operation of the self-timed memory (column 18, lines 6 – 12), and the external clock signal to the internal memory block during a test mode of the self-timed memory (column 19, lines 5 – 10), wherein providing the external clock signal to the at least one internal memory block comprises providing the external clock signal to a plurality of different internal memory blocks (column 4, lines 10 – 18). Churchill does not explicitly teach: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal; and detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test mode of the self-timed memory; and a predetermined test pattern to provide the external clock signal.

Irrinki teaches: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal (column 4, lines 13 – 15; claim 2).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill: a method for providing an external clock signal to an internal memory block of a self-timed memory comprising receiving an internal clock signal and receiving an external clock signal with the teaching of Irrinki: an external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal for the purpose of performing propagation delay measurements (column 3, lines 39 – 46). Propagation delay testing is well known in the art (column 3, lines 39 – 46). Modification of the duty cycle of an external clock signal is well known in art for the purpose of propagation delay testing (column 4, lines 10 – 24). One of

ordinary skill in the art, at the time of the invention, would have recognized that applying the known technique to the known device would have yielded a predictable result.

Savir teaches: detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test mode of the self-timed memory (column 1, lines 10 – 30).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill: a method for providing an external clock signal to an internal memory block of a self-timed memory comprising receiving an internal clock signal and receiving an external clock signal with the teaching of Savir: detecting a slow-to-rise delay or a slow-to-fall delay for the purpose of device testing (column 1, lines 10 – 36). Slow-to-rise (STR) and slow-to-fall (STF) fault testing is well known technique in the art. One of ordinary skill in the art, at the time of the invention, would have recognized that applying the known technique to the known device would have yielded a predictable result.

Lackey teaches: a predetermined test pattern providing the external clock signal to a plurality of different internal blocks (column 5, lines 61 – 65; column 6, lines 10 – 16).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill: a method for providing an external clock signal to an internal memory block of a self-timed memory comprising receiving an internal clock signal and receiving an external clock signal with the teaching of Lackey: a predetermined test pattern providing the external clock signal to a plurality of different

internal blocks for the purpose of isolating clock domains during testing (column 2, lines 7 – 52). Predetermined test pattern for enabling internal clocks is a well known technique in the art. One of ordinary skill in the art, at the time of the invention, would have recognized that applying the known technique to the known device would have yielded a predictable result. And for the reasons stated above the claim is rejected.

7. Regarding claim 3, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 1. Churchill additionally teaches: the delay circuit programmed for generating an internal clock with a duty cycle less then 50% (column 17, lines 33 – 50). Churchill additionally teaches: an external clock with a configurable duty cycle (column 19, lines 5 – 10). Churchill does not explicitly teach: the duty cycle of the external clock signal received during test mode comprising a duty cycle lower than a 50% duty cycle typical for operation of the at least one internal memory block.

Irrinki teaches: the duty cycle of the external clock signal received during test mode comprising a duty cycle lower than a 50% duty cycle typical for operation of the at least one internal memory block (column 3, lines 39 – 46). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

8. Regarding claim 4, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 1. Churchill additionally teaches: the duty cycle of the external clock signal received during test mode comprises a duty cycle higher than a 50% duty cycle typical for operation of the at least one internal memory block (column 18, lines 46 – 48;

column 19, lines 5 – 10). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

9. Regarding claim 5, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 1. Churchill additionally teaches: providing internal clock signal to the at least one internal memory block in an absence of the control signal (column 19, lines 5 – 10). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

10. Regarding claim 6, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 1. Churchill additionally teaches: receiving a control signal indicating initiation of the test mode (column 19, lines 5 – 10). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

11. Regarding claim 7, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 6. Churchill additionally teaches: receiving a control signal indicating termination of the test mode (column 19, lines 5 – 10). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

12. Regarding claim 8, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 7. Churchill additionally teaches: receiving the control signal during

the test mode (column 19, lines 5 – 10). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

13. Regarding claim 9, Churchill teaches: A self-timed memory (figure 2) comprising: at least one internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218); a clock monitor (figure 9, 902) for receiving an external clock signal (figure 2, clk) and for providing a clock signal (figure 9, element 902) to the at least one internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218); a test system (figure 9, element 908, 910) interposed between the clock monitor (figure 9, 902) and the at least one internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218). The test system comprising: an internal clock signal input port (figure 9, element 908) in signal communication with the clock monitor for receiving an internal clock signal (figure 9, element 916); an external clock signal input port (figure 9, element 910) for receiving the external clock signal (figure 9, element 914); a control signal input port (figure 9, element 908) for receiving a control signal (figure 9, element 912); an output port in signal communication with the at least one internal memory block (figure 2, element 222); and a multiplexer in signal communication with the internal clock signal input port, the external clock signal input port, the control signal input port, and the output port (figure 9, element 908, 910); wherein the multiplexer is configured to receive the internal clock signal, the external clock signal, and the control signal; and wherein the multiplexer is further configured to provide, in dependence upon the control signal, the internal clock signal via the output port to the internal memory block during a normal

mode of operation of the self-timed memory (column 18, lines 6 – 12), and the external clock signal to the internal memory block during a test mode of the self-timed memory (column 19, lines 5 – 10), wherein providing the external clock signal to the at least one internal memory block comprises providing the external clock signal to a plurality of different internal memory blocks (column 4, lines 10 – 18). Churchill does not explicitly teach: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal; detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the at least one internal memory block during the test mode of the self-timed memory, and a predetermined test pattern to provide the external clock signal.

Irrinki teaches: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal (column 4, lines 13 – 15; claim 2).

Savir teaches: detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the at least one internal memory block during the test mode of the self-timed memory (column 1, lines 10 – 30).

Lackey teaches: a predetermined test pattern providing the external clock signal to a plurality of different internal blocks (column 5, lines 61 – 65; column 6, lines 10 – 16). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

14. Regarding claim 10, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 9. Churchill additionally teaches: the clock monitor comprises an

input port for receiving the external clock signal (figure 9, element 902, signal 914) and wherein the input port is connected to the external clock signal input port of the test system (figure 9, element 908. 910, signal 914). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

15. Regarding claim 11, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 10. Churchill additionally teaches: test circuitry in signal communication with the test system (figure 2, element 212), the test circuitry for providing the control signal to the test system and for providing the external clock signal to the test system during the test mode (column 5, lines 13 – 25).

16. Regarding claim 12, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 9. Churchill additionally teaches: the at least one internal memory block comprises an address decoder (figure 2, element 204, 208). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

17. Regarding claim 13, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 9. Churchill additionally teaches: the at least one internal memory block comprises a sense amplifier (figure 2, element 214). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

18. Regarding claim 16, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 9. Churchill additionally teaches: the at least one internal memory block comprises input/output latches (figure 2, element 216, 218). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

19. Regarding claim 17, Churchill teaches: A self-timed memory (figure 2) comprising: at least one internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218); a clock monitor (figure 9, 902) for receiving an external clock signal (figure 2, clk) and for providing a clock signal (figure 9, element 902) to the at least one internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218); a test system (figure 9, element 908, 910) interposed between the clock monitor (figure 9, 902) and the at least one internal memory block(figure 2, element 202, 204, 206, 208, 214, 216, 218). The test system comprising: an internal clock signal input port (figure 9, element 908) in signal communication with the clock monitor for receiving an internal clock signal (figure 9, element 916); an external clock signal input port (figure 9, element 910) for receiving the external clock signal (figure 9, element 914); a control signal input port (figure 9, element 908) for receiving a control signal (figure 9, element 912); an output port in signal communication with the at least one internal memory block (figure 2, element 222); and control circuitry in signal communication with the internal clock signal input port, the external clock signal input port, the control signal input port and the output port (figure 9, element 908, 910); wherein the control circuitry is configured to receive the internal clock signal, the external clock signal, and the control signal; and

wherein the control circuitry is further configured to provide, in dependence upon the control signal, the internal clock signal via the output port to the at least one internal memory block during a normal mode of operation of the self-timed memory (column 18, lines 6 – 12), and for providing the external clock signal to the at least one internal memory block during a test mode of the self-timed memory (column 19, lines 5 – 10), wherein providing the external clock signal to the at least one internal memory block comprises providing the external clock signal to a plurality of different internal memory blocks (column 4, lines 10 – 18). Churchill does not explicitly teach: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal; detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the at least one internal memory block during the test mode of the self-timed memory; and a predetermined test pattern to provide the external clock signal.

Irrinki teaches: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal (column 4, lines 13 – 15; claim 2).

Savir teaches: detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the at least one internal memory block during the test mode of the self-timed memory (column 1, lines 10 – 30).

Lackey teaches: a predetermined test pattern providing the external clock signal to a plurality of different internal blocks (column 5, lines 61 – 65; column 6, lines 10 – 16). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

20. Regarding claim 18, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 17. Churchill additionally teaches: the control circuitry comprises a multiplexer (figure 9, element 908, 910). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

21. Regarding claim 19, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 18. Churchill additionally teaches: the at least one internal memory block comprises an address decoder (figure 2, element 204, 208). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

22. Regarding claim 20, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 19. Churchill additionally teaches: the at least one internal memory block comprises a sense amplifier (figure 2, element 214). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

23. Claims 14, 15, and 21 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill, Irrinki, Savir, and Lackey, in view of Choi, U.S. Patent 6,324,115 (herein Choi).

24. Regarding claim 14, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 9. Churchill additionally teaches: the at least one internal

memory block comprising a column decoder (figure 2, 208). Churchill does not explicitly teach: the at least one internal memory block comprising a bank decoder.

Choi teaches: at least one internal memory block comprising a bank decoder (figure 1, element 160).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an internal memory block, and a column decoder, as cited above, with the teaching of Choi, a bank decoder, for the purpose of addressing memory (column 1, lines 19 – 27). A self-timed memory is a well known device in the art. A bank decoder for addressing internal memory blocks is a well known technique (column 1, lines 38 – 41). One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded the predictable result of addressable memory (abstract).

25. Regarding claim 15, Churchill, Irrinki, Savir, and Lackey teach the limitations of the parent claim, claim 9. Churchill teaches the limitations of the parent claim, claim 9. Churchill does not explicitly teach: the at least one internal memory block comprising a precharge and discharge circuitry.

Choi teaches: the at least one internal memory block comprising a precharge and discharge circuitry (figure 1, element 310, 320).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an

internal memory block, as cited above, with the teaching of Choi, precharge and discharge circuitry. A self-timed memory is a well known device in the art. Precharge and discharge circuitry for accessing internal memory blocks is a well known technique (column 2, lines 51 – 58). One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded predictable the predictable result of addressable memory (abstract).

26. Regarding claim 21, Churchill, Irrinki, Savir, Lackey, and Choi teach the limitations of the parent claim, claim 20. Churchill additionally teaches: the internal memory block comprising a column decoder (figure 2, 208). Churchill does not explicitly teach: the at least one internal memory block comprising a bank decoder.

Choi teaches: an at least one internal memory block comprising a bank decoder (figure 1, element 160).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an internal memory block, and a column decoder, as cited above, with the teaching of Choi; a bank decoder, for the purpose of addressing memory (column 1, lines 19 – 27). A self-timed memory is a well known device in the art. A bank decoder for addressing internal memory blocks is a well known technique (column 1, lines 38 – 41). One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded predictable the predictable result of addressable memory (abstract).

27. Regarding claim 22, Churchill, Irrinki, Savir, Lackey, and Choi teach the limitations of the parent claim, claim 21. Churchill teaches the limitations of the parent claim, claim 9. Churchill does not explicitly teach: the at least one internal memory block comprising a precharge and discharge circuitry.

Choi teaches: the at least one internal memory block comprising a precharge and discharge circuitry (figure 1, element 310, 320).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an internal memory block, as cited above, with the teaching of Choi; precharge and discharge circuitry. A self-timed memory is a well known device in the art. Precharge and discharge circuitry for accessing internal memory blocks is a well known technique (column 2, lines 51 – 58). One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded predictable the predictable result of addressable memory (abstract).

28. Regarding claim 23, Churchill, Irrinki, Savir, Lackey, and Choi teach the limitations of the parent claim, claim 22. Churchill additionally teaches: the at least one internal memory block comprises input/output latches (figure 2, element 216, 218). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

29. Regarding claim 24, Churchill, Irrinki, Savir, Lackey, and Choi teach the limitations of the parent claim, claim 23. Churchill additionally teaches: test circuitry in signal communication with the test system (figure 2, element 212), the test circuitry for providing the control signal to the test system and for providing the external clock signal to the test system during the test mode (column 5, lines 13 – 25). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

Conclusion

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL F. MCMAHON whose telephone number is (571)270-3232. The examiner can normally be reached on M-Th 8am-5pm(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffery Gaffin can be reached on (571) 272-4146. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dfm
11/29/10

/Robert W. Beausoliel, Jr./
Supervisory Patent Examiner, Art Unit 2113